CASCADING ANALOG AND DIGITAL NOISE FIGURES

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INTRODUCTION

The use of DSP in wireless receivers was initially limited to modem algorithms and other forms of baseband processing. The whole radio from RF to baseband was analog and the channel selection was performed using analog filters. This type of receiver is still common and has the advantage that an AGC (Automatic Gain Control) loop can be used to establish a strong signal level at the input of the A/D converter. As a result, the noise contribution from the DSP sub-system is not critical for the performance of the receiver and is typically included in the required E_b/N_0 rather than in the receiver noise figure. However, in the new generation of digitized, multi-standard wireless receivers, both the A/D converter and the DSP have moved into the radio domain and *out of* the AGC loop, thereby becoming significant contributors to the system noise figure. From the radio architect's perspective, the DSP sub-system is now just like any other part of the radio; it must be assigned a noise figure and included in the receiver noise budget where it becomes a part of the total receiver noise figure.

In an accompanying paper [1], we defined the noise figure of a DSP system and described how the digital noise figure concept can be used in the design of DSP solutions for wireless receivers. The noise figure of a DSP system was found to be a function of the bitwidths along the signal path. We illustrated this by calculating the noise figure of two common DSP structures, a decimation filter and a CORDIC rotator, as well as a more complex system, a digital down-converter (DDC). In this follow-up paper, we extend our analysis to systems comprised of both analog and digital processing blocks. The A/D converter now becomes the focal point, because it is here that the need arises to cascade (combine) an analog noise figure with its digital counterpart. Consequently, we begin by deriving the noise figure of an A/D converter cascaded with a DDC. It is shown that the A/D converter parameters have a fundamental influence on the degree by which the DDC affects the cascaded noise figure. A case study is then presented in which we evaluate an RF-sampled receiver design for the IEEE 802.22 standard

and also discuss several ways of improving the receiver performance by "tuning" the parameters of the A/D-DDC cascade.

NOISE IN DSP SYSTEMS

In the first white paper [1], the properties of noise in DSP systems were discussed at some length, and for the sake of continuity a brief summary is given here. As before, our focus is on *custom* DSP, i.e. algorithm-specific solutions for ASIC or FPGA. All signal samples and filter coefficients are assumed to be 2's complement integers, and the term "bitwidth" refers to the word length at a specific point in the signal path (the bitwidth often varies considerably along the signal path). Noise appears in a DSP system when the bitwidth at some point in the signal path is truncated by an operation that discards a number of the least significant bits (LSBs). However, instead of straight-forward truncation, *rounding* is often used in order to avoid a negative bias (DC offset) in the signal. A rounding method that completely eliminates the bias is said to be *convergent*. Figure 1 depicts the mathematical model of a convergent round operation that deletes n bits. It is seen that the round operation acts as an attenuator followed by an additive noise source. Under normal circumstances, the noise samples generated by the round operation will form a stationary white process with power spectral density (PSD) as shown in Figure 1b. Further, all noise (error) values except the two boundary values (±0.5) will occur with equal probability, as illustrated in Figure 1c.

The probability mass function in Figure 1c can be used to calculate the power (i.e. the mean square value) of the round-off noise as a function of the number of discarded bits n [1]. Except for very small values of n, the result is approximately 1/12 and the approximation improves quickly with increasing n. Since there is really no reason to use a round operation that only removes a small number of bits, we can safely adopt a model where all round operations in the system generate precisely the same amount of noise power 1/12. This fixed amount of power gets distributed along a frequency axis that extends from 0 to $f_s/2$, resulting in a PSD given by

$$\eta_0 = \frac{1}{6f_s} = \frac{T_s}{6} \quad [\mathrm{Hz}^{-1}] \tag{1}$$

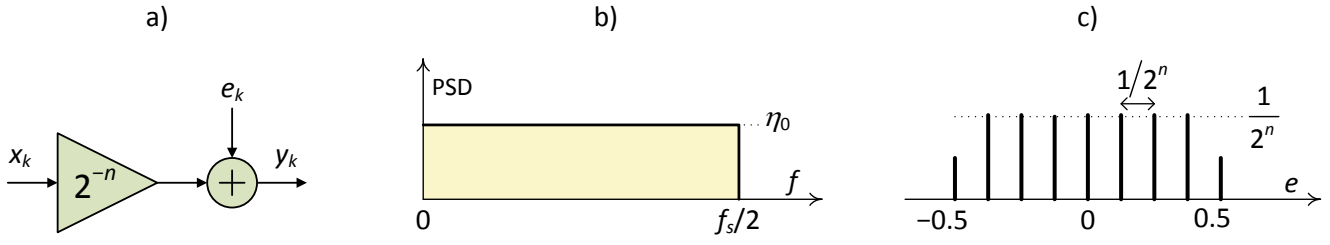

Figure 1 Mathematical representation of rounding. a) Equivalent model. b) Power spectral density of round-off noise. c) Probability mass function of round-off noise (n = 3).

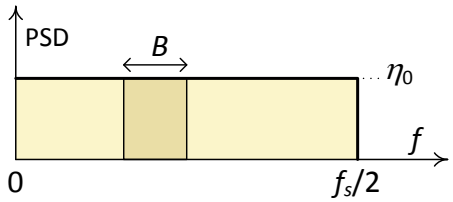

Figure 2 Only the portion of the round-off noise that falls within the user's bandwidth is relevant.

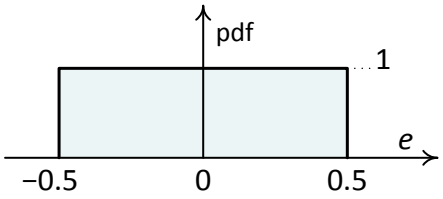

Figure 3 Probability density function of ideal quantization noise.

and $T_s = 1/f_s$ is the sample period. Since power is dimensionless in the digital domain, power spectral density has dimension 1/Hz, or seconds. For a DSP system designer, the PSD level in Eq. (1) is of fundamental importance, because it determines the amount of noise power that falls within the bandwidth occupied by the user signal, as illustrated in Figure 2. Furthermore, this PSD applies not only to round-off noise, but also to the quantization noise in an A/D converter. Ideal quantization noise has the probability density function shown in Figure 3. The mean square value of this probability density function also evaluates to 1/12, which means that the PSD of ideal quantization noise is the same as for round-off noise. In fact, *any* digital (i.e. quantized) waveform with uncorrelated quantization noise will exhibit a noise floor with PSD given by Eq. (1).

Noise Figure in the Analog and Digital Domains

The noise figure of a system, whether it is analog or digital, can generally be defined as the degradation of SNR experienced by a signal as it passes through the system. Figure 4a shows the basic setup used to define noise figure in the analog domain [2] [3]. The device-under-test (DUT) is a two-port connected to a signal source and a load. The SNR is measured at both the input and the output, across the user bandwidth *B*. Because of the noise generated within the DUT, the output SNR will always be less than the input SNR. This degradation of SNR is measured by the *noise factor*, defined as

$$F = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} \tag{2}$$

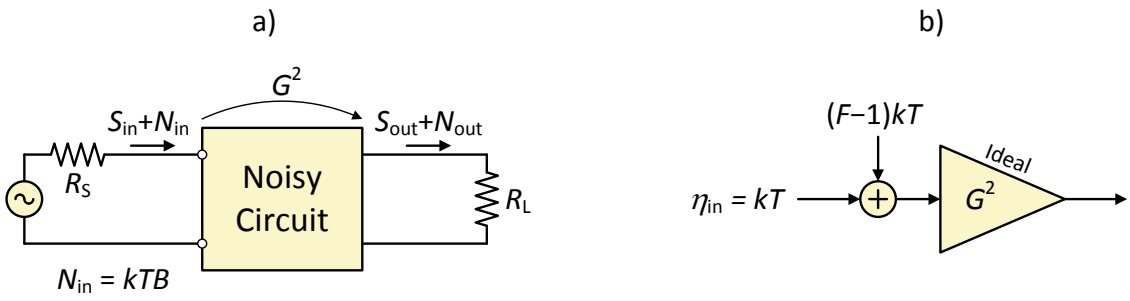

Figure 4 Noise figure in the analog domain. a) Basic setup. b) Equivalent system model with input-referred excess noise PSD.

We will find it convenient to distinguish between noise factor, given in linear scale, and *noise figure*, denoted by *NF*, which is the noise factor expressed in dB. Note that the noise factor definition requires that the input (source) noise level N_{in} is specified; without an *input noise level reference*, the definition is ambiguous. When working with the noise factor of an analog system, input impedance matching is usually assumed, i.e. the source resistance is assumed to equal the input resistance of the two-port. The matched condition leads to $N_{in} = kTB$, where k is Boltzmann's constant and T is the temperature in degrees Kelvin, usually taken to be 290° K.

The noise factor of a DSP system can be defined in essentially the same way, as shown in Figure 5a. Power in the digital domain must of course be interpreted as mean square value, a dimensionless quantity since digital samples have no dimension. As for the input noise level, the obvious choice is to use the PSD in Eq. (1), the "inescapable" noise floor in digital systems. Hence, the input noise power is in this case defined as $N_{in} = T_s B/6$, where T_s is the sample period at the system input. With these modifications, Eq. (2) can be used as a definition of noise figure in the digital domain.

Other than serving as definition of noise figure, Eq. (2) is not particularly useful. To actually calculate the noise figure, a simpler expression is needed. We begin by writing $S_{out}/S_{in} = G^2$, where G^2 is the power gain of the DUT. Note that G is defined here as the square root of the power gain, which is the convention in DSP systems but differs from the convention in RF systems (when living in both worlds, certain compromises are unavoidable). Further, by letting η_{in} and η_{out} denote the input and output noise PSD in the user frequency band, we obtain $N_{out}/N_{in} = (\eta_{out}B)/(\eta_{in}B) = \eta_{out}/\eta_{in}$, where $\eta_{in} = kT$ for an analog system and $\eta_{in} = T_s/6$ for a digital system. Using these results, the noise factor in Eq. (2) can be written as

$$F = \frac{\eta_{out}}{G^2 \eta_{in}} \tag{3}$$

Next, we note that there are two principal noise sources contributing to the noise level at the output of the DUT, namely the noise originating from the input and the noise generated inside the DUT. The latter is commonly known as the *output-referred excess noise*. Letting η_{ex} denote the PSD of the output-referred excess noise, the noise factor can now be expressed as

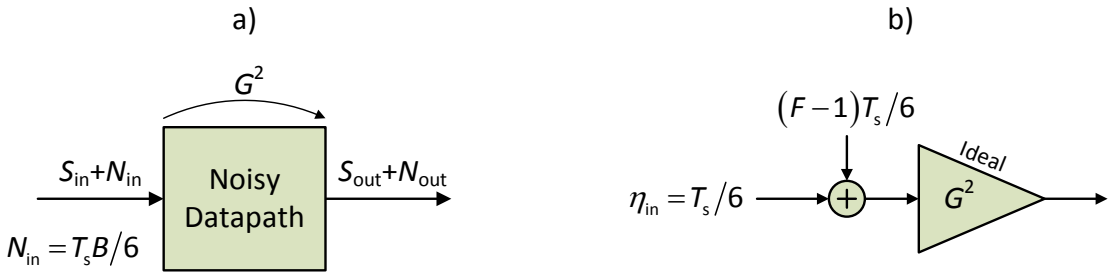

Figure 5 Noise figure in the digital domain. a) Basic setup. b) Equivalent system model with input-referred excess noise PSD.

$$F = \frac{G^2\eta_{in} + \eta_{ex}}{G^2\eta_{in}} = 1 + \frac{\eta_{ex}}{G^2\eta_{in}} \tag{4}$$

Conversely, if the noise factor has already been calculated, the equation above can be used to solve for the output excess noise level, given by

$$\eta_{ex} = G^2(F-1)\eta_{in} \tag{5}$$

It is often convenient to think of the excess noise as being generated by a fictitious noise source located at the input of an ideal (noiseless) system, as shown in Figure 4b for an analog system and Figure 5b for a digital system. This theoretical noise source, with PSD given by $\eta_{ex}/G^2 = (F-1)\eta_{in}$, is referred to as the *input-referred excess noise*. Notice that since the input noise level η_{in} is a known quantity, the input-referred excess noise level is completely specified by the noise factor.

The above results apply to both analog and digital systems; it is merely a matter of defining the input noise level η_{in} as either kT or $T_s/6$. However, for the remainder of this section we will focus on the digital domain. An appropriate starting point is to calculate the noise factor of the single round operation in Figure 1. The excess noise PSD generated by a single round operation is of course $\eta_{ex} = T_s/6$ and the gain is $G = 2^{-n}$, where n is the number of discarded bits. Substituting into Eq. (4), we immediately get

$$F = 1 + \frac{T_s/6}{\left(2^{-n}\right)^2 T_s/6} = 1 + 4^n \tag{6}$$

Notice that the noise factor depends on the number of discarded bits, even though the power in the noise source does not.

A slightly more complicated case is depicted in Figure 6. This is a very common DSP structure: a noiseless signal path with sample rate conversion, followed by a single round operation. Decimation and interpolation filters of both FIR (Finite Impulse Response) type and CIC (Cascaded Integrator Comb) type are often designed this way. Let us define the *rate conversion factor* of the system as $R = f_{s,out}/f_{s,in} = T_{s,in}/T_{s,out}$, which means that $R < 1$ for a decimator and $R > 1$ for an interpolator. Again the only contributor to the output excess noise is the round operation at the output. This gives

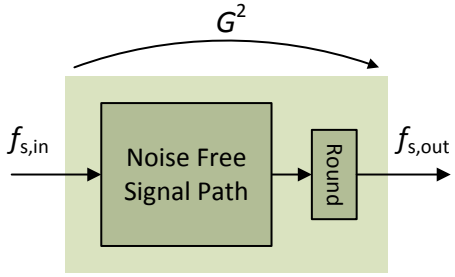

Figure 6 DSP system with one round operation.

$$F = 1 + \frac{T_{s,out}/6}{G^2 T_{s,in}/6} = 1 + \frac{1}{G^2 R} \tag{7}$$

In [1] we observed that for practically every type of DSP block (not just the one in Figure 6), the gain can be written as

$$G = \gamma \cdot 2^{w_{\text{out}} - w_{\text{in}}} \tag{8}$$

where w_{in} and w_{out} are the input and output bitwidths, and γ is a constant that is algorithm-dependent but independent of w_{in} and w_{out}. In most cases it is necessary to keep $\gamma \leq 1$, since the signal gain, when expressed in bits, cannot exceed the bitwidth expansion inside the block without risk of overflow. However, there are exceptions; when strong interfering signals outside the user band are rejected by a filter, this may create a signal headroom in the datapath that allows γ to be increased beyond 1 without risk of non-linear behavior.

Substituting the gain in Eq. (8) into the noise factor formula in Eq. (7), we obtain the noise factor

$$F = 1 + \frac{1}{\left(\gamma 2^{w_{\text{out}} - w_{\text{in}}}\right)^2 R} = 1 + \frac{1}{\gamma^2 R} \cdot 4^{w_{\text{in}} - w_{\text{out}}} \tag{9}$$

Observe that the noise factor expression is on the general form

$$F = 1 + K_{\text{F}} \cdot 4^{w_{\text{in}} - w_{\text{out}}} \tag{10}$$

As discussed in [1], virtually every linear DSP algorithm defined in integer arithmetic can be designed so that the noise factor takes this form. We see that the noise factor can be made to approach 1, equivalent to a noiseless system, by increasing the difference between the input and output bitwidths. Notice also that letting $K_F = 1$ in Eq. (10) gives the noise factor of a single round operation (see Eq. (6)). Is it possible to have $K_F < 1$, thereby obtaining a noise factor that is less than that of a round operation? It certainly is, in the case of an interpolating filter, i.e. a filter with $R > 1$. For example, we can see this

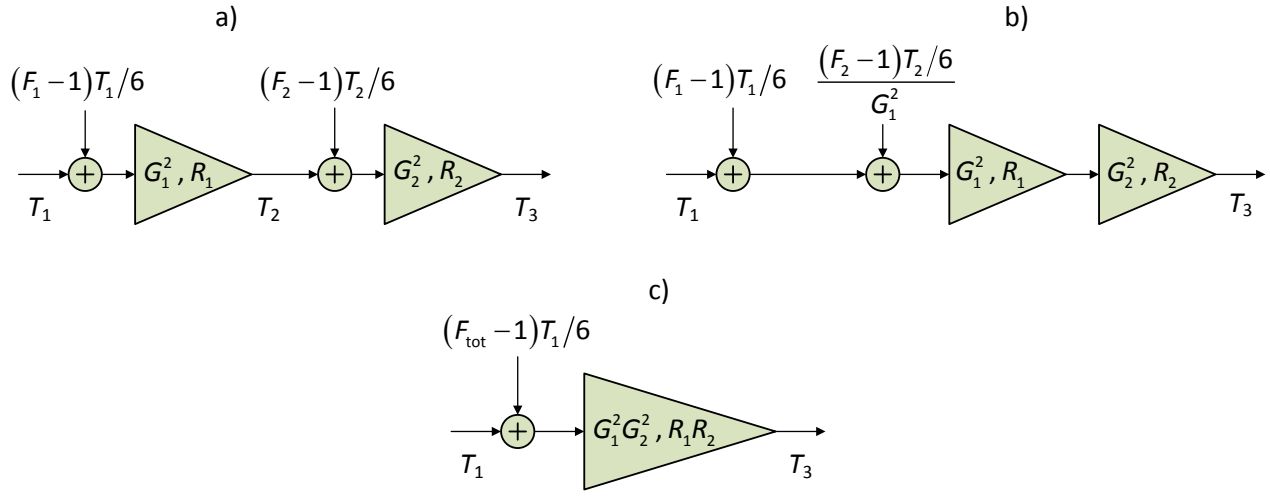

Figure 7 Combining the noise factors of two DSP blocks.

by looking at the noise factor in Eq. (9), where $K_F = 1/(\gamma^2 R)$.

So far we have focused on the calculation of noise factors for individual processing blocks. To calculate the noise factor of a more complex digital system, we must also be able to combine the noise factors of cascaded blocks into a single noise factor. Consider the cascade of two DSP blocks in Figure 7a with sample periods T_1, T_2 and T_3. In order to obtain the total noise figure for this cascade, we first refer the excess noise in block 2 to the input of block 1, as shown in Figure 7b, and then merge the two noise sources into one. Next, we express the resulting noise level in terms of a new noise factor F_{tot}, as illustrated in Figure 7c. The result is

$$F_{tot} = F_1 + \frac{(F_2 - 1)}{G_1^2 R_1} \tag{11}$$

where $R_1 = T_1/T_2$ is the rate conversion factor of the first DSP block. Not surprisingly, in the special case $R_1 = 1$ this becomes the well known formula for combining noise factors in the analog domain.

As an application of Eq. (11), consider calculating the noise figure of the simple digital down-converter (DDC) in Figure 8. The signal path in the DDC consists of a CORDIC phase-rotation block [4] serving as a complex synthesizer/mixer, two Cascaded Integrator Comb (CIC) decimation stages [5] with decimation factor 3, a low-order FIR filter to compensate for the passband droop in the two CIC filters [6], and two FIR decimation stages [5] with decimation factor 2. Taken together, the four decimation stages achieves a decimation factor of 3·3·2·2 = 36. The CORDIC rotator block, in combination with the phase accumulator, acts as both a synthesizer and a mixer, down-converting the desired user signal to baseband by phase-rotating the input samples. Table 1 lists the gains, rate conversion factors and noise figures of the individual DSP blocks in the DDC. The cascaded (cumulative) noise figures, calculated using Eq. (11), are listed in the last column. For example, the cascaded noise figure of the CORDIC rotator and the first decimation stage is 6.13 dB, and the total cascaded noise figure of the whole DDC is 11.94 dB. For more information about the design of this DDC, see [1]. Note that the input sample rate does not need to be specified. The DDC noise figure is a function of the parameters in the signal path, including the rate conversion factors in the decimation stages, but not the clock frequency of the system.

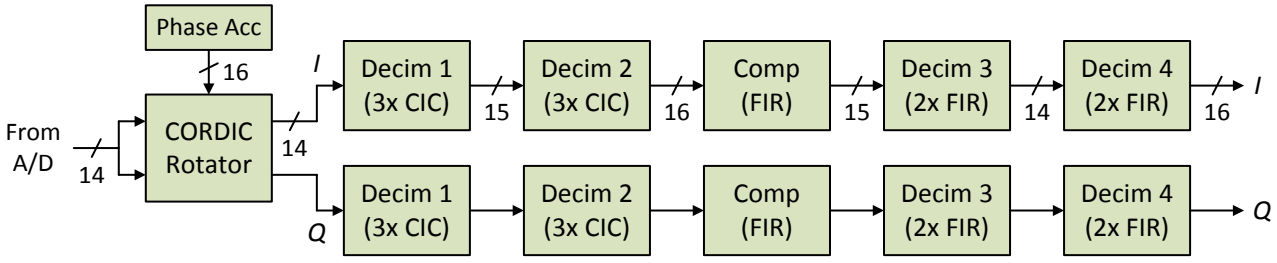

Figure 8 Digital Down-Converter.

Table 1 Parameter Settings for the Digital Down-Converter in Figure 8.

Block	w_{in}	w_{out}	Gain [dB]	Rate Conv	*NF* [dB]	Cascaded *NF* [dB]
CORDIC	14	14	−1.69	1	4.07	4.07
Decim 1	14	15	4.54	1/3	3.12	6.13
Decim 2	15	16	11.59	1/3	0.82	6.46
Comp Filter	16	15	−10.10	1	10.51	8.89
Decim 3	15	14	−0.24	1/2	4.93	11.68
Decim 4	14	16	11.96	1/2	0.52	11.94
DDC Total	14	16	16.06	1/36	11.94	

CASCADING ANALOG AND DIGITAL NOISE FIGURES

Thus far, we have treated analog and digital noise figure as two separate entities. Now it is time for the two to meet. Our objective in this section is to derive the noise figure of the system in Figure 9, which consists of a DDC in cascade with an A/D converter running at sampling rate $f_{AD} = 1/T_{AD}$. The number of bits in the A/D converter is n_{AD}, the input voltage range is ±Vp and the input terminating resistance is R_{AD}. Because the A/D converter has an analog input, it can be modeled as in Figure 4 and characterized by an analog noise figure. Contributing to this noise figure is the analog noise from the A/D front-end (buffer and sample-and-hold circuit) as well the quantization noise from the encoder section. Here we will find it convenient to express the A/D noise figure as a function of the *effective number of bits* in the A/D converter, denoted n_{eff}. The effective number of bits (ENOB) is the number of bits it would take to produce an ideal quantization noise level equal to the actual noise level in the A/D. For the sake of argument, we will ignore the non-linear distortion in the A/D converter, which is normally included in the ENOB [7]. We can then equate the input-referred excess noise PSD of the A/D, given by $(F_{AD} - 1)kT$, with the noise PSD generated by an ideal quantizer with quantization step $q_{eff} = V_p / 2^{n_{eff}-1}$ Volts. The total noise power generated by such a quantizer is $q_{eff}^2 / 12 / R_{AD}$ Watts, distributed over a bandwidth of $f_{AD}/2$ Hz. This gives

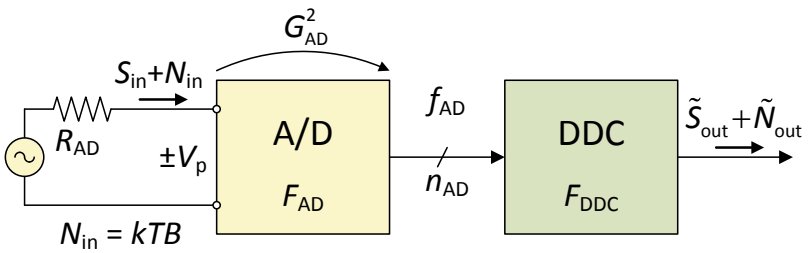

Figure 9 Cascaded A/D converter and DDC.

$$(F_{AD}-1)kT = \frac{q_{eff}^2/12/R_{AD}}{f_{AD}/2} = \frac{V_p^2/R_{AD}}{3/2\cdot 2^{2n_{eff}}\cdot f_{AD}} \tag{12}$$

By using the approximation $F_{AD}-1 \approx F_{AD}$ and converting to logarithmic scale, the A/D noise figure can now be written as

$$NF = \underbrace{\left(V_p^2/R_{AD}\right)_{dBm}}_{\text{A/D peak input power}} - 1.76 - 6.02n_{eff} - 10\log_{10} f_{AD} + 174 \tag{13}$$

We see that the noise figure is limited by the A/D peak input power, the number of effective bits and the sampling rate. Observe that the first term really is the *peak* power, not the maximum RMS power. In a wideband receiver, the RMS power at the A/D input is usually far below the peak power, due to the fact that the input signal is a superposition of many carriers and therefore has a very high peak-to-average ratio.

Again consider the A/D-DDC cascade in Figure 9. Since the full-scale input voltage V_p generates a digital value of $2^{n_{AD}-1}$, we can define a "power gain" for the A/D converter, given by

$$g_{AD}^2 = \frac{2^{2(n_{AD}-1)}}{V_p^2/R_{AD}} \quad [\mathrm{W}^{-1}] \tag{14}$$

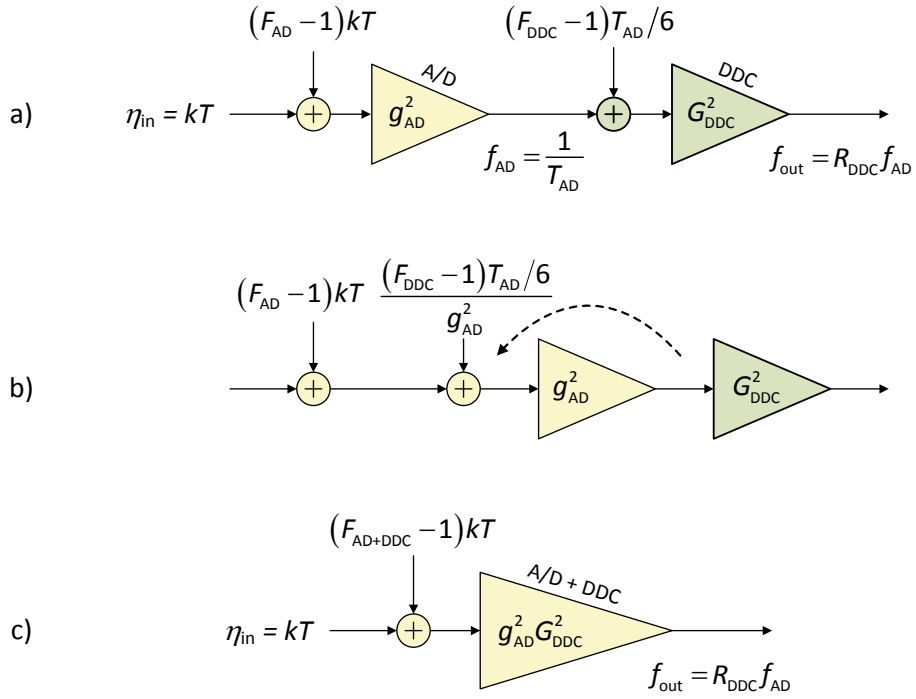

Figure 10 Combining A/D and DDC noise factors.

The gain in Eq. (14) has unit 1/W since we are going from analog power measured in Watts to dimensionless power (mean square value) in the digital domain. In Figure 9, the signal and noise power at the output of the DDC sub-system are denoted by $\tilde{S}_{out}$ and $\tilde{N}_{out}$ to emphasize that these are dimensionless quantities defined in the digital domain. Nevertheless, a noise level that exists in the digital domain can always be *referred* to the input of the A/D converter, i.e. it can be thought of as being generated by a fictitious analog noise source located at the A/D input. Once the digital excess noise has been referred to the A/D input in this way, it can be merged with the input-referred excess noise of the A/D converter itself and the total noise level can be expressed using a new noise figure. To do this, we model the cascaded A/D and DDC sub-systems as shown Figure 10a. The two noise factors can now be combined by first referring the input excess noise of the DDC to the input of the A/D converter, as illustrated in Figure 10b, summing the two noise sources and finally expressing the resulting noise PSD in terms of a new *analog* noise factor F_{AD+DDC}:

$$\left(F_{AD+DDC}-1\right)kT = \left(F_{AD}-1\right)kT + \frac{\left(F_{DDC}-1\right)T_{AD}/6}{g_{AD}^2} = \left(F_{AD}-1+\frac{\left(F_{DDC}-1\right)T_{AD}/6}{g_{AD}^2 kT}\right)kT \tag{15}$$

Comparing the first and last equalities, we find that

$$F_{AD+DDC} = F_{AD} + \frac{\left(F_{DDC}-1\right)T_{AD}/6}{g_{AD}^2 kT} \tag{16}$$

This is the desired result, but it would be more convenient to combine the two noise factors using the traditional formula

$$F_{AD+DDC} = F_{AD} + \frac{F_{DDC}-1}{G_{AD}^2} \tag{17}$$

with some appropriate definition of G_{AD}^2. Comparing Eqs. (16) and (17), we see that this is indeed possible if we define

$$G_{AD}^2 = g_{AD}^2 \frac{kT}{T_{AD}/6} \tag{18}$$

Note that although the factor G_{AD}^2 acts as a power gain in Eq. (17), its only real use is in combining the analog and digital noise factors. We refer to G_{AD}^2 as the *cascading gain* of the A/D converter. As can be seen in Eq. (18), the cascading gain accounts for the fact that we are merging two noise factors that are based on different noise references. The cascading gain can be expressed as the ratio of *kT*, the analog noise reference level at the A/D input, and $T_{AD}/6/g_{AD}^2$, the digital noise reference level *referred to the same point in the signal path* (the A/D input). We can gain even more insight by substituting the power gain in Eq. (14) into the cascading gain in Eq. (18) and converting to logarithmic scale. The result is

$$\left(G_{AD}^2\right)_{dB} = 1.76 + 6.02n_{AD} + 10\log_{10} f_{AD} - \left(V_p^2/R_{AD}\right)_{dBm} - 174 \quad (19)$$

This equation, in combination with cascading formula in Eq. (17), shows how the basic parameters of the A/D converter affect the DDC contribution to the total noise figure. As seen from Eq. (17), even a small DDC noise figure can have a big impact on the total noise figure if the A/D cascading gain is insufficient. Also notice that the cascading gain depends on the actual number of bits n_{AD}, whereas the A/D noise figure in Eq. (13) depends on the effective number of bits n_{eff}. Apart from this, the cascading gain and the A/D noise figure are functions of the same parameters, but with opposite sign. In fact, we can combine Eqs. (19) and (13) to obtain

$$\left(G_{AD}^2\right)_{dB} = 6.02\left(n_{AD} - n_{eff}\right) - NF_{AD} \quad (20)$$

Now, if our objective is to improve the receiver noise figure by making a parameter change in the A/D converter, then the above equation is the bearer of good news. It tells us that a change in the A/D converter parameters aimed at reducing the A/D noise figure is also likely to increase the A/D cascading gain, thereby reducing the contribution from the DDC noise figure (again, see Eq. (17)). The exception occurs when an increase in the effective number of bits n_{eff} is achieved, e.g. by improving the S/H circuit design, without changing the actual number of bits n_{AD}. In this case, the A/D noise figure is improved but the noise contribution from the DDC remains the same.

However, viewed from a different perspective, Eq. (20) is bad news. Suppose that our objective is to "push complexity out of the mixed-signal domain and into the digital domain". That is, we wish to reduce the complexity of the A/D converter (the number of bits or the sampling frequency), which is bound to degrade the A/D noise figure, and then compensate by using more digital hardware resources to achieve a lower DDC noise figure. Ideally, the reduction in the DDC noise figure should compensate for the increase in the A/D noise figure, keeping the overall noise figure unchanged. Unfortunately, the equation above tells us that any such attempt is futile. As soon as we increase the A/D noise figure, we decrease the A/D cascading gain, which in turn increases the degree by which the DDC contributes to the total noise figure. It is certainly possible to reduce the DDC noise figure by using more digital hardware, but this improvement in the DDC noise figure is likely to be cancelled by the drop in the cascading gain. The result is a net increase of the total noise figure. We can conclude that although it is certainly possible to shift complexity from the mixed-signal domain to the digital domain, it is very difficult to do so without degrading the total noise figure.

Another conclusion that can be drawn from Eq. (20) is that for many A/D converters, the cascading gain expressed in dB will be negative. High-speed A/D converters typically have noise figures well over 20 dB, which means that the actual number of bits in the A/D converter must exceed the effective number of bits by 3.5 or more before the cascading gain can turn positive. To compensate for a negative A/D cascading gain, the DDC must be designed with a noise figure that is significantly smaller than that of the A/D converter.

CASE STUDY: AN RF-SAMPLING RECEIVER FOR 802.22

In this section, we apply the results derived above to the design of an RF-sampled receiver based on the new IEEE 802.22 standard [8]. This standard defines a wireless system for unlicensed operation in the VHF and UHF bands using vacant TV channels, so called "white spaces". Because of the favorable propagation conditions in these bands, the 802.22 system is designed to support communication over a range of up to 100 km and is classified as a Wireless Regional Area Network (WRAN). The 802.22 waveform is based on OFDM modulation [9] and is designed to fit within a TV channel. The standard actually defines three different versions of this waveform, in order to support TV channels with bandwidths 6, 7, and 8 MHz. Our focus here is on the United States, where the TV channel bandwidth is 6 MHz. Most of the TV channels in the United States (channels 14 – 51) are clustered in a frequency band extending from 470 to 698 MHz. The present receiver is designed to use a subset of these channels, namely channels 21 – 35, which occupy the frequency band from 512 to 602 MHz. Consequently, the receiver must support a bandwidth of 90 MHz.

Figure 11 shows a basic breakdown of the receiver. It consists of an analog front-end with 20 dB of conversion gain and a noise figure of 5 dB, an A/D converter running at 246.816 Msps and the DDC shown in Figure 8 with parameters as in Table 1. Note that there is no mixer in the analog front end; the radio signal, after filtering and amplification, is fed directly to the A/D converter. Channel selection is handled entirely by the DDC. The desired output sample rate from the DDC is 6.856 MHz, since this is the sample rate at which the OFDM modem will operate in an 802.22 system with 6 MHz channel

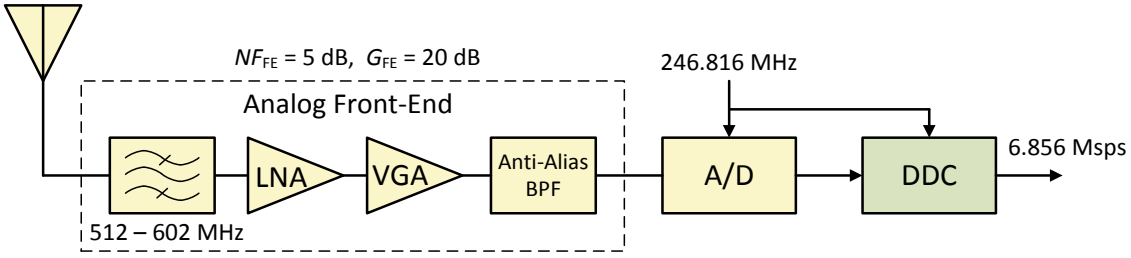

Figure 11 RF-sampling receiver for the 802.22 WRAN system.

Table 2 Fixed A/D Parameter Settings.

Sampling Rate (f_{AD})	246.816 MHz
Peak Input Voltage (V_p)	0.9 V
Input Resistance (R_{AD})	200 Ω
Peak Input Power	6.1 dBm
Analog Bandwidth	> 602 MHz

bandwidth. To simplify the DDC, the A/D sampling rate was constrained to be an integer multiple of the desired output rate. A multiple of 36 was chosen, both because this multiple can be factored into simple prime numbers (thus leading to simple decimation filters) and because the resulting A/D frequency, given by 36·6.856 MHz = 246.816 MHz, does not generate any harmonics inside the receive band.

The objective of this case study is to evaluate the total noise figure of the 802.22 receiver outlined above for various A/D and DDC configurations, while holding the gain and noise figure of the analog front-end constant. Some A/D parameters, specified in Table 2, will also be held constant. The targeted noise figure for an 802.22 receiver is generally in the range 6 – 10 dB. Note in Table 2 that the A/D peak input power is fixed at 6.1 dBm. If the signal peak power at the A/D input were to exceed this limit, the A/D converter would be driven into saturation. This means that with a front-end gain of 20 dB, the signal peak power at the receiver input must not exceed 6.1 – 20 = −13.9 dBm. Higher power levels can be handled by switching out some of the gain in the analog front-end (hence the VGA indicated in Figure 11), albeit for the price of a degraded noise figure. However, here we will assume that the front-end gain stays fixed at 20 dB.

Figure 12 shows the A/D-DDC configuration of the first system, “System 1”. Here a 14-bit A/D converter is interfaced directly to the DDC in Figure 8. The effective number of bits achieved by the A/D converter is 11.5, which corresponds to a noise figure of 25.2 dB (calculated using Eq. (13)). To obtain the total receiver noise factor F_{RX}, we first combine the A/D and DDC noise factors using Eq. (17) and then apply the usual formula to cascade the A/D-DDC noise factor with the noise factor of the analog front-end:

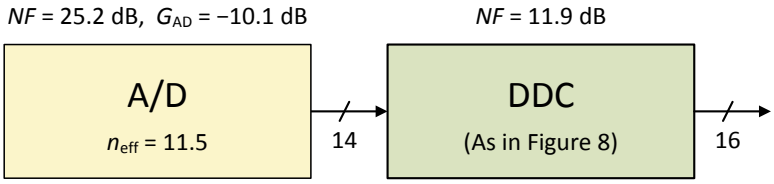

Figure 12 A/D-DDC sub-system (System 1).

Table 3 Gains and Noise Figures of System 1.

Sub-System	Gain [dB]		Noise Figure [dB]	
Analog Front-End	20.0		5.0	
A/D Converter	−10.1	6.0	25.2	26.8
DDC	16.1		11.9	
Receiver Total	26.0		9.0	

$$F_{RX} = F_{FE} + \frac{F_{AD+DDC} - 1}{G_{FE}^2} \tag{21}$$

The results for System 1 are summarized in Table 3. The combined noise figure of the A/D and the DDC is 26.8 dB, which yields a total receiver noise figure of 9.0 dB when cascaded with the 5.0 dB noise figure in the front-end. Note that the gain specified for the A/D converter (−10.1 dB) is the *cascading* gain given by Eq. (19). As already mentioned, it is common for an A/D converter to have a negative cascading gain, which is why the DDC noise figure generally has to be significantly smaller than the A/D noise figure. To get a better idea of how much the DDC contributes to the combined A/D-DDC noise figure, we can compare the two terms in the cascading formula of Eq. (17). The A/D noise figure is 25.2 dB whereas the "boosted" DDC noise figure, given by $(F_{DDC} - 1)/G_{AD}^2$, is 21.8 dB. The conclusion is that the A/D noise figure dominates but the DDC noise figure is a significant contributor.

There is more than one way to improve the noise figure in System 1. However, as long as the DDC contributes significantly to the total noise figure, investing more digital hardware to reduce the DDC noise figure will likely be the most cost-effective solution. A complete re-design of the DDC will achieve this, but there is another approach that can accomplish the same thing with a much smaller effort. In [1], we discussed the technique of *scaling* a datapath to reduce the noise figure. Figure 13 shows the A/D-DDC configuration of System 2, which uses this approach. The A/D converter is the same as before, but all signal bitwidths inside the DDC have been incremented by 1. Scaling, by itself, will not change the noise figure of the DCC. Recall that both the gain and the noise figure of a DSP block are

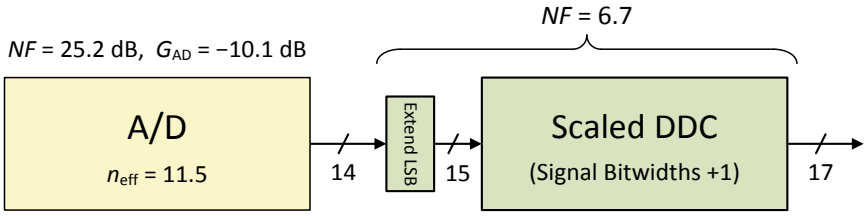

Figure 13 A/D-DDC sub-system (System 2).

Table 4 Gains and Noise Figures of System 2.

Sub-System	Gain [dB]		Noise Figure [dB]	
Analog Front-End	20.0		5.0	
A/D Converter	−10.1	12.0	25.2	25.6
DDC	22.1		6.7	
Receiver Total	32.0		8.3	

functions of the *difference* between its input and output bitwidths, as indicated by Eqs. (8) and (10). Consequently, incrementing all signal bitwidths will have no affect on the gains and noise figures of the individual blocks in the DDC and therefore no affect on the total DDC noise figure. However, the expansion of the DDC input bitwidth from 14 to 15 makes it possible to scale the samples from the A/D converter by a factor of 2 before they enter the DDC, as shown in Figure 13. In hardware, this is done by simply appending a new (zero) LSB to each sample, an operation we refer to as 'Extend LSB'. Adding a 6 dB gain to the input of the DDC has a dramatic effect on its noise factor. We can calculate this noise factor by using the formula for cascaded digital noise factors in Eq. (11). The noise factor of the 'Extend LSB' operation is 1 since this operation does not add any noise. The old DDC noise factor is 15.63 (11.94 dB). This gives a new DDC noise factor of

$$\tilde{F}_{\text{DDC}} = 1 + \frac{(15.63-1)}{2^2} = 4.66 \tag{22}$$

which corresponds to a noise figure of 6.7 dB. We have thus managed to reduce the DDC noise figure by roughly 5.3 dB. The improvement comes with a price tag, of course. As discussed in [1], we can expect the hardware sizes in the DDC, including the amount of combinational logic and register storage, to grow by roughly 7% when the bitwidths in the datapath are increment by one. Table 4 summarizes the gains and noise figures of System 2. With the modified DDC, the noise figure of the A/D-DDC sub-system becomes 25.6 dB. Cascaded with the 5.0 dB noise figure in the analog front-end, this gives a total receiver noise figure of 8.3 dB. The A/D noise figure is still 25.2 dB, but the DDC contribution term $(F_{\text{DDC}}-1)/G_{\text{AD}}^2$ in the cascading formula has shrunk to 15.7 dB. From Table 4 we see

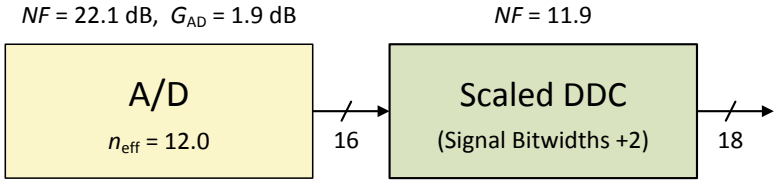

Figure 14 A/D-DDC sub-system (System 3).

Table 5 Gains and Noise Figures of System 3.

Sub-System	Gain [dB]		Noise Figure [dB]	
Analog Front-End	20.0		5.0	
A/D Converter	1.9	18.0	22.1	22.4
DDC	16.1		11.9	
Receiver Total	38.0		6.9	

that the DDC now only adds a few tenths of a dB to the combined A/D-DDC noise figure. We can continue to scale the DDC datapath in the same fashion, but the small additional improvement may not be worth the extra hardware. For example, incrementing the signal bitwidths in the DDC by two, while scaling the input samples by a factor of 4 (12 dB), yields a DDC noise figure of 2.8 dB and a combined A/D-DDC noise figure of 25.3 dB. The resulting receiver noise figure is 8.15 dB, a very small improvement.

It is clear that to take the system performance to the next level, we will need to change some of the A/D parameters. In System 3, depicted in Figure 14, the A/D converter has been upgraded to 16 bits. The new A/D converter achieves an effective bitwidth of 12.0, which corresponds to a noise figure of 22.1 dB. For an A/D converter running at 246 MHz with an analog bandwidth of over 600 MHz, this can be said to represent the state of the art at the time of this writing. To interface the DDC to the new 16-bit A/D, the DDC datapath must be scaled by incrementing all signal bitwidths by two. Observe that this is only done to allow the DDC to accept the 16-bit data from the A/D; there is no improvement of the DDC noise figure, which remains at 11.9 dB. However, with $n_{AD} - n_{eff} = 4$, the new A/D converter actually achieves a positive cascading gain of 1.9 dB, as can be seen in Table 5. This has the same effect as reducing the DDC noise figure. As a result, the DDC noise figure is now attenuated rather than boosted in the cascading formula and its effect on the total noise figure is almost negligible. The combined A/D-DDC noise figure is 22.4 dB, only 0.3 dB above the A/D noise figure, and the total receiver noise figure has dropped to 6.9 dB.

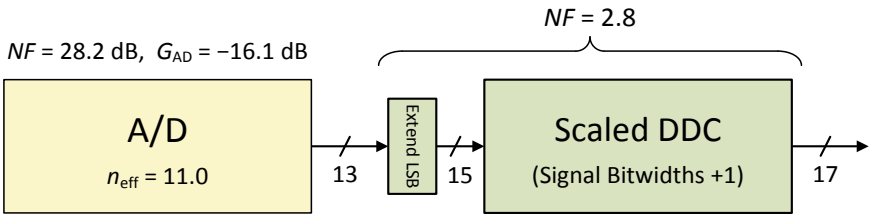

Figure 15 A/D-DDC sub-system (System 4).

Table 6 Gains and Noise Figures of System 4.

Sub-System	Gain [dB]		Noise Figure [dB]	
Analog Front-End	20.0		5.0	
A/D Converter	−16.1	12.0	28.2	28.4
DDC	28.1		2.8	
Receiver Total	32.0		10.0	

Earlier in this paper we discussed the possibility of shifting complexity from the mixed-signal domain to the digital domain. The conclusion was that this is very hard to do without degrading the overall noise figure. We now use System 4, depicted in Figure 15, to exemplify this. In this system the A/D converter has been downgraded to 13 bits. The effective number of bits achieved by the A/D converter is 11.0, corresponding to a noise figure of 28.2 dB. This is a high noise figure, but it gets worse. Substituting $n_{AD} = 13$ into Eq. (19), we find that the cascading gain has now dropped to −16.1 dB, significantly boosting the contribution of the DCC noise. What can be done to remedy this situation? Because the data coming from the A/D converter is now 13 bits, we could use the existing DDC, which has a 14-bit input, with an 'Extend LSB' operation placed in front of it. We already know that the noise figure of the DDC (scaled or not) cascaded with a 6 dB gain at the input is 6.7 dB. However, in this case we need to do even better. By incrementing all the signal bitwidths in the DDC by one, thus obtaining a DDC with a 15-bit input, and using the 'Extend LSB' operation at the input to append two LSBs, we end up with a 12 dB gain before the DDC. As mentioned earlier, this DDC configuration has a noise figure of 2.8 dB. Table 6 gives the gains and noise figures of System 4. We see that when the 28.2 dB noise figure of the A/D converter is cascaded with the 2.8 dB noise figure of the DDC using a combining gain of −16.1 dB, the result is an A/D-DDC noise figure of 28.4 dB. Hence, by using a modified DDC with a very low noise figure, we have managed to eliminate the impact of the DDC on the cascaded noise figure almost completely. This is as good as it gets. Nevertheless, the total receiver noise figure has grown to 10.0 dB, just barely acceptable for an 802.22 receiver.

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